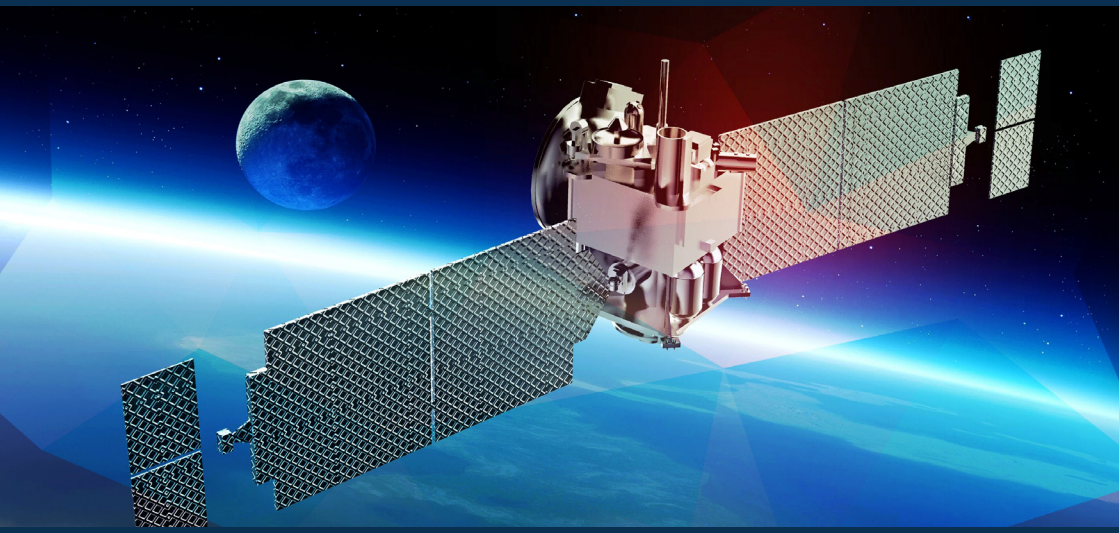
NELSON MANDELA UNIVERSITY

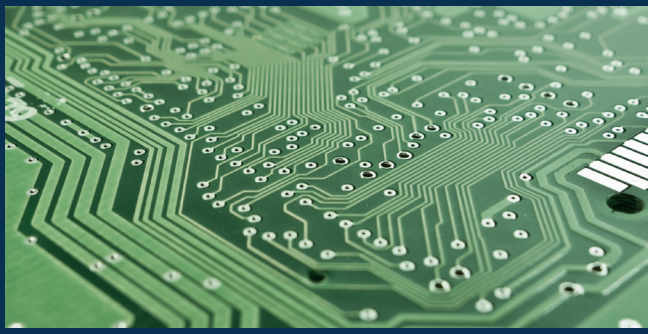
Innovation Office



Space Radiation

Digital electronic circuits, both Application Specific Integrated Circuits (ASICs) as well as programmable digital logic circuits are subject to interference caused by radiation resulting in errors, known as Single Event Transients (SETs) and Single Event Upsets (SEUs). SETs and SEUs are known to occur in electronics used in space aircraft and other applications and can lead to effects that may or may not permanently damage circuitry.

The invention is a SET suppression circuit for non-volatile FPGAs and ASICs. It is able to detect and correct more efficiently as well as consumes less space on the circuit board than traditional solutions.



Advantages

- Mitigates effects of SET and SEU in FPGAs and ASICs
- Can suppress SET effects regardless of input state
- Setup allows for correction of error
- Less complexity, spatial overhead and power than conventional SET suppression methods

Market Application

Telecommunications and aerospace industries.

Opportunities

- Investment
- Partnership
- Distribution
- Manufacturing
- Licenses

Development Status

TRL 5: early prototype stage. The Radiation Mitigation VHDL Coding Technique of the prototype has been tested in space aboard the SCS Space nSight1 satellite.

IP Protection

Granted patents in the United States of America and South Africa.

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